Public Works and Government Services Canada

Travaux publics et Services gouvernementaux Canada

RETURN BIDS TO:
RETOURNER LES SOUMISSIONS À:

Bid Receiving Public Works and Government Services Canada/Réception des soumissions Travaux publics et Services gouvernementaux Canada
Pacific Region
401 - 1230 Government Street
Victoria, B.C.
V8W 3X4
Bid Fax: (250) 363-3344

REQUEST FOR PROPOSAL
DEMANDE DE PROPOSITION

Proposal To: Public Works and Government Services Canada

We hereby offer to sell to Her Majesty the Queen in right of Canada, in accordance with the terms and conditions set out herein, referred to herein or attached hereto, the goods, services, and construction listed herein and on any attached sheets at the price(s) set out therefor.

Proposition aux: Travaux Publics et Services Gouvernementaux Canada

Nous offrons par la présente de vendre à Sa Majesté la Reine du chef du Canada, aux conditions énoncées ou incluses par référence dans la présente et aux annexes ci-jointes, les biens, services et construction énumérés ici sur toute feuille ci-annexée, au(x) prix indiqué(s).

Comments - Commentaires

Title - Sujet
POWER MX MODELLING & BOARD DESIGN

Solicitation No. - N° de l'invitation	**Date**
31034-143415/B	2014-06-18

Client Reference No. - N° de référence du client
31034-143415

GETS Reference No. - N° de référence de SEAG
PW-$VIC-211-6495

File No. - N° de dossier	**CCC No./N° CCC - FMS No./N° VME**
VIC-4-37022 (211)	

Solicitation Closes - L'invitation prend fin
at - à 02:00 PM
on - le 2014-07-04

Time Zone
Fuseau horaire
Pacific Daylight Saving Time PDT

F.O.B. - F.A.B.
Plant-Usine: ☐ **Destination:** ☑ **Other-Autre:** ☐

Address Enquiries to: - Adresser toutes questions à:	**Buyer Id - Id de l'acheteur**
Park, Isabell	vic211

Telephone No. - N° de téléphone	**FAX No. - N° de FAX**
(250) 363-3981 ( )	(250) 363-3344

Destination - of Goods, Services, and Construction:
Destination - des biens, services et construction:
NATIONAL RESEARCH COUNCIL CANADA
717 WHITE LAKE ROAD
KALEDEN
BRITISH COLUMBIA
V0H1K0
CANADA

Instructions: See Herein

Instructions: Voir aux présentes

Vendor/Firm Name and Address
Raison sociale et adresse du fournisseur/de l'entrepreneur

Delivery Required - Livraison exigée	**Delivery Offered - Livraison proposée**
See Herein	

Vendor/Firm Name and Address
Raison sociale et adresse du fournisseur/de l'entrepreneur

Telephone No. - N° de téléphone
Facsimile No. - N° de télécopieur

Name and title of person authorized to sign on behalf of Vendor/Firm (type or print)
Nom et titre de la personne autorisée à signer au nom du fournisseur/ de l'entrepreneur (taper ou écrire en caractères d'imprimerie)

Signature **Date**

Issuing Office - Bureau de distribution
Public Works and Government Services Canada - Pacific Region
401 - 1230 Government Street
Victoria, B. C.
V8W 3X4

Canada

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PART 1 - GENERAL INFORMATION

1. Introduction

The bid solicitation document is divided into six parts plus attachments and annexes as follows:

Part 1 General Information: provides a general description of the requirement;
Part 2 Bidder Instructions: provides the instructions, clauses and conditions applicable to the bid solicitation;
Part 3 Bid Preparation Instructions: provides bidders with instructions on how to prepare their bid;
Part 4 Evaluation Procedures and Basis of Selection: indicates how the evaluation will be conducted, the evaluation criteria that must be addressed in the bid, and the basis of selection;
Part 5 Certifications: includes the certifications to be provided; and
Part 6 Resulting Contract Clauses: includes the clauses and conditions that will apply to any resulting contract.

The Annexes include the Statement of Work, the Basis of Payment and any other annexes.

2. Summary

NRC requires a research and development services in support of the international Square Kilometer Array (SKA). https://www.skatelescope.org

Contractors bidding on his requirement must meet the required delivery dates as these are essential towards Canada meeting its deliverables towards the set timelines of the SKA project office.

Bidders must provide a list of names, or other related information as needed, pursuant to section 01 of Standard Instructions 2003.

2.1 Reissue of Bid Solicitation

This bid solicitation cancels and supersedes previous bid solicitation number 31034-143415/A dated 2014-05-13 with a closing of 2014-05-29 at 2:00pm PDT. A debriefing or feedback session will be provided upon request to bidders/offerors/suppliers who bid on the previous solicitation.

3. Debriefings

After contract award, bidders may request a debriefing on the results of the bid solicitation process. Bidders should make the request to the Contracting Authority within 15 working days of receipt of the results of the bid solicitation process. The debriefing may be in writing, by telephone or in person.

4. Communications

As a courtesy and in order to coordinate any public announcements pertaining to this contract, the Government of Canada requests that successful Bidders notify the Contracting Authority 5 days in advance of their intention to make public an announcement related to the recommendation of a contract award, or any information related to the contract. The Government of Canada retains the right to make primary contract announcements.

5. Conflict of Interest

The Work described herein and the deliverable items under any resulting Contract specifically exclude the development of any statement of work, evaluation criteria or any document related to a bid solicitation. The Contractor, its subcontractor(s) or any of their agent(s) directly or indirectly involved in the performance of the Work and/or in the production of the deliverables under any resulting Contract will not be precluded from bidding on any potential future bid solicitation related to the production or exploitation of any concept or prototype developed or delivered under any resulting Contract.

PART 2 - BIDDER INSTRUCTIONS

1. Standard Instructions, Clauses and Conditions

All instructions, clauses and conditions identified in the bid solicitation by number, date and title are set out in the *Standard Acquisition Clauses and Conditions Manual* (*https://buyandsell.gc.ca/policy-and-guidelines/standard-acquisition-clauses-and-conditions-manual)* issued by Public Works and Government Services Canada.

Bidders who submit a bid agree to be bound by the instructions, clauses and conditions of the bid solicitation and accept the clauses and conditions of the resulting contract.

The 2003 (2014-03-01) Standard Instructions - Goods or Services - Competitive Requirements, are incorporated by reference into and form part of the bid solicitation.

2. Submission of Bids

Bids must be submitted only to Public Works and Government Services Canada (PWGSC) Bid Receiving Unit by the date, time and place indicated on page 1 of the bid solicitation.

3. Former Public Servant

Contracts awarded to former public servants (FPS) in receipt of a pension or of a lump sum payment must bear the closest public scrutiny, and reflect fairness in the spending of public funds. In order to comply with Treasury Board policies and directives on contracts awarded to FPS, bidders must provide the information required below before contract award. If the answer to the questions and, as applicable the information required have not been received by the time the evaluation of bids is completed, Canada will inform the Bidder of a time frame within which to provide the information. Failure to comply with Canada's request and meet the requirement within the prescribed time frame will render the bid non-responsive.

Definitions

For the purposes of this clause,"former public servant" is any former member of a department as defined in the *Financial Administration Act*, R.S., 1985, c. F-11, a former member of the Canadian Armed Forces or a former member of the Royal Canadian Mounted Police. A former public servant may be:

a. an individual;
b. an individual who has incorporated;
c. a partnership made of former public servants; or
d. a sole proprietorship or entity where the affected individual has a controlling or major interest in the entity.

"lump sum payment period" means the period measured in weeks of salary, for which payment has been made to facilitate the transition to retirement or to other employment as a result of the implementation of various programs to reduce the size of the Public Service. The lump sum payment period does not include the period of severance pay, which is measured in a like manner.

"pension" means a pension or annual allowance paid under the *Public Service Superannuation Act* (PSSA), R.S., 1985, c.P-36, and any increases paid pursuant to the *Supplementary Retirement Benefits Act*, R.S., 1985, c.S-24 as it affects the PSSA. It does not include pensions payable pursuant to the *Canadian Forces Superannuation Act*, R.S., 1985, c.C-17, the *Defence Services Pension Continuation Act*, 1970, c.D-3, the *Royal Canadian Mounted Police Pension Continuation Act* , 1970, c.R-10, and the *Royal Canadian Mounted Police Superannuation Act*, R.S., 1985, c.R-11, the *Members of Parliament Retiring Allowances Act* , R.S., 1985, c.M-5, and that portion of pension payable to the *Canada Pension Plan Act*, R.S., 1985, c.C-8.

Former Public Servant in Receipt of a Pension

As per the above definitions, is the Bidder a FPS in receipt of a pension? **Yes** ( ) **No** ( )

If so, the Bidder must provide the following information, for all FPS in receipt of a pension, as applicable:

a. name of former public servant;
b. date of termination of employment or retirement from the Public Service.

By providing this information, Bidders agree that the successful Bidder's status, with respect to being a former public servant in receipt of a pension, will be reported on departmental websites as part of the published proactive disclosure reports in accordance with Contracting Policy Notice: 2012-2 and the Guidelines on the Proactive Disclosure of Contracts.

Work Force Adjustment Directive
Is the Bidder a FPS who received a lump sum payment pursuant to the terms of the Work Force Adjustment Directive? **Yes** ( ) **No** ( )

If so, the Bidder must provide the following information:

a. name of former public servant;
b. conditions of the lump sum payment incentive;
c. date of termination of employment;
d. amount of lump sum payment;
e. rate of pay on which lump sum payment is based;
f. period of lump sum payment including start date, end date and number of weeks;
g. number and amount (professional fees) of other contracts subject to the restrictions of a work force adjustment program.

For all contracts awarded during the lump sum payment period, the total amount of fees that may be paid to a FPS who received a lump sum payment is $5,000, including Applicable Taxes.

4. Communications - Solicitation Period
All enquiries must be submitted to the Contracting Authority no later than 5 calendar days before the bid closing date. Enquiries received after that time may not be answered.

Bidders should reference as accurately as possible the numbered item of the bid solicitation to which the enquiry relates. Care should be taken by bidders to explain each question in sufficient detail in order to enable Canada to provide an accurate answer. Technical enquiries that are of a "proprietary" nature must be clearly marked "proprietary" at each relevant item. Items identified as proprietary will be treated as such except where Canada determines that the enquiry is not of a proprietary nature. Canada may edit the question(s) or may request that the Bidder do so, so that the proprietary nature of the question(s) is eliminated and the enquiry can be answered to all bidders. Enquiries not submitted in a form that can be distributed to all bidders may not be answered by Canada.

5. Applicable Laws
Any resulting contract must be interpreted and governed, and the relations between the parties determined, by the laws in force in British Columbia.

Bidders may, at their discretion, substitute the applicable laws of a Canadian province or territory of their choice without affecting the validity of their bid, by deleting the name of the Canadian province or territory specified and inserting the name of the Canadian province or territory of their choice. If no change is made, it acknowledges that the applicable laws specified are acceptable to the bidders.

6. Improvement of Requirement During Solicitation Period
Should bidders consider that the specifications or Statement of Work contained in the bid solicitation could be improved technically or technologically, bidders are invited to make suggestions, in writing, to the Contracting Authority named in the bid solicitation. Bidders must clearly outline the suggested improvement as well as the reason for the suggestion. Suggestions that do not restrict the level of competition nor favour a particular bidder will be given consideration provided they are submitted to the

Contracting Authority at least 5 days before the bid closing date. Canada will have the right to accept or reject any or all suggestions.

7. Basis for Canada's Ownership of Intellectual Property

The National Research Council Canada has determined that any intellectual property rights arising from the performance of the Work under the resulting contract will belong to Canada, on the following grounds:

- the main purpose of the contract, or of the deliverables contracted for, is to augment an existing body of Canada's background information as a prerequisite to the transfer of the augmented background to the private sector, through licensing or assignment of ownership (not necessarily to the original contractor), for the purposes of commercial exploitation;
- the main purpose of the contract, or of the deliverables contracted for, is to deliver a component or subsystem that will be incorporated into a complete system at a later date, as a prerequisite to the planned transfer of the complete system to the private sector, through licensing or assignment of ownership, for purposes of commercial exploitation.

PART 3 - BID PREPARATION INSTRUCTIONS

1. Bid Preparation Instructions
Canada requests that bidders provide their bid in separately bound sections as follows:

Section I : Technical Bid (1hard copies)
Section II : Financial Bid (1 hard copies)
Section III : Certifications (1 hard copies)

If there is a discrepancy between the wording of the soft copy and the hard copy, the wording of the hard copy will have priority over the wording of the soft copy.

Prices must appear in the financial bid only. No prices must be indicated in any other section of the bid.

Bidders can bid on more than one stream of work specified in Annex A, but should submit one separate bid for each specified stream of work. Canada requests that bidders clearly identify in the first pages of their bid which stream of work they are bidding on.

Canada requests that bidders follow the format instructions described below in the preparation of their bid:

(a) use 8.5 x 11 inch (216 mm x 279 mm) paper; and
(b) use a numbering system that corresponds to the bid solicitation.

In April 2006, Canada issued a policy directing federal departments and agencies to take the necessary steps to incorporate environmental considerations into the procurement process Policy on Green Procurement (http://www.tpsgc-pwgsc.gc.ca/ecologisation-greening/achats-procurement/politique-policy-eng.html). To assist Canada in reaching its objectives, bidders should:

(1) use paper containing fibre certified as originating from a sustainably-managed forest and containing minimum 30% recycled content; and

(2) use an environmentally-preferable format including black and white printing instead of colour printing, print double sided/duplex, using staples or clips instead of cerlox, duotangs or binders.

Section I : Technical Bid
In their technical bid, bidders should demonstrate their understanding of the requirements contained in the bid solicitation and explain how they will meet these requirements. Bidders should demonstrate their capability and describe their approach in a thorough, concise and clear manner for carrying out the work.

The technical bid should clearly address and in sufficient depth the points that are subject to the evaluation criteria against which the bid will be evaluated. Simply repeating the statement contained in the bid solicitation is not sufficient. In order to facilitate the evaluation of the bid, Canada requests that bidders address and present topics in the order of the evaluation criteria under the same headings. To avoid duplication, bidders may refer to different sections of their bids by identifying the specific paragraph and page number where the subject topic has already been addressed.

Section II : Financial Bid

1.1 Bidders must submit their financial bid in accordance with the following:

(a) A firm, all inclusive lot price for the Work. The total amount of Applicable Tax is to be shown separately, if applicable.

(b) For Canadian-based bidders, prices must be in Canadian funds, Applicable Taxes excluded and Canadian customs duties and excise taxes included.

For foreign-based bidders, prices must be in Canadian funds, Applicable Taxes, Canadian customs duties and excise taxes excluded. Canadian customs duties and excise taxes payable by Canada will be added, for evaluation purposes only, to the prices submitted by foreign-based bidders.

For the purpose of the bid solicitation, bidders with an address in Canada are considered Canadian-based bidders and bidders with an address outside of Canada are considered foreign-based bidders.

Section III : Certifications
Bidders must submit the certifications required under Part 5.

PART 4 - EVALUATION PROCEDURES AND BASIS OF SELECTION

1. Evaluation Procedures

(a) Bids will be assessed in accordance with the entire requirement of the bid solicitation including the technical and financial evaluation criteria.

(b) An evaluation team composed of representatives of Canada will evaluate the bids.

1.1 Technical Evaluation

The technical bid should address clearly and in sufficient depth the points that are subject to the evaluation criteria against which the bid will be evaluated. Simply repeating the statement contained in the bid solicitation is not sufficient. In order to facilitate the evaluation of the bid, Canada requests that bidders address and present topics in the order of the evaluation criteria under the same headings. To avoid duplication, bidders may refer to different sections of their bids by identifying the specific paragraph and page number where the subject topic has already been addressed.

1.1.1 Supporting Information

In the event that the Bidder fails to submit any supporting information pursuant to mandatory technical criteria, the Contracting Authority may request it thereafter in writing, including after the closing date of the bid solicitation. It is mandatory that the Bidder provide the supporting information within three (3) business days of the written request or within such period as specified or agreed to by the Contracting Authority in the written notice to the Bidder.

1.1.2 Mandatory Technical Criteria

Refer to Attachment A, Mandatory Technical Criteria.

1.1.3 Delivery Date Request

MEX4 project:
While delivery is requested by August 31, 2014, the best delivery that could be offered is _____.

P32S project:
While delivery is requested by August 31, 2014, the best delivery that could be offered is _____.

1.2 Financial Evaluation

1.2.1 Evaluation of Price

The price of the bid will be evaluated in Canadian dollars, Applicable Taxes excluded, Canadian customs duties and excise taxes included.

2. Basis of Selection

2.1 Basis of Selection - Lowest Evaluated Price

A bid must comply with the requirements of the bid solicitation and meet all mandatory technical evaluation criteria to be declared responsive. The responsive bid with the lowest evaluated price per project will be recommended for award of contracts.

PART 5 - CERTIFICATIONS

Bidders must provide the required certifications and documentation to be awarded a contract.

The certifications provided by bidders to Canada are subject to verification by Canada at all times. Canada will declare a bid non-responsive, or will declare a contractor in default, if any certification made by the Bidder is found to be untrue, whether made knowingly or unknowingly, during the bid evaluation period or during the contract period.

The Contracting Authority will have the right to ask for additional information to verify the Bidder's certifications. Failure to comply and to cooperate with any request or requirement imposed by the Contracting Authority may render the bid non-responsive or constitute a default under the Contract.

1. Certifications Required Precedent to Contract Award

1.1 Integrity Provisions – Associated Information

By submitting a bid, the Bidder certifies that the Bidder and its Affiliates are in compliance with the provisions as stated in Section 01 Integrity Provisions - Bid of Standard Instructions 2003. The associated information required within the Integrity Provisions will assist Canada in confirming that the certifications are true.

1.2 Federal Contractors Program for Employment Equity - Bid Certification

By submitting a bid, the Bidder certifies that the Bidder, and any of the Bidder's members if the Bidder is a Joint Venture, is not named on the Federal Contractors Program (FCP) for employment equity "FCP Limited Eligibility to Bid" list (http://www.labour.gc.ca/eng/standards_equity/eq/emp/fcp/list/inelig.shtml) available from Employment and Social Development Canada (ESDC) - Labour's website

Canada will have the right to declare a bid non-responsive if the Bidder, or any member of the Bidder if the Bidder is a Joint Venture, appears on the "FCP Limited Eligibility to Bid"list at the time of contract award.

PART 6 - RESULTING CONTRACT CLAUSES

The following clauses and conditions apply to and form part of any contract resulting from the bid solicitation.

1. Statement of Work
The Contractor must perform the Work in accordance with the Statement of Work at Annex A.

2. Standard Clauses and Conditions
All clauses and conditions identified in the Contract by number, date and title are set out in the *Standard Acquisition Clauses and Conditions* Manual (https://buyandsell.gc.ca/policy-and-guidelines/standard-acquisition-clauses-and-conditions-manual) issued by Public Works and Government Services Canada.

2.1 General Conditions
2035 (2014-03-01), General Conditions - Higher Complexity - Services, apply to and form part of the Contract.

2.2 Supplemental General Conditions
The following supplemental general conditions apply to and form part of the Contract:

4007 (2010-08-16), Canada to Own Intellectual Property Rights in Foreground Information

3. Security Requirement
There is no security requirement applicable to this Contract.

4. Term of Contract

4.1 Delivery Date
All the deliverables must be received on or before _____.

5. Authorities

5.1 Contracting Authority
The Contracting Authority for the Contract is:

Name: Ji-Yon Isabell Park
Title: Supply Specialist
Public Works and Government Services Canada
Acquisitions Branch
Telephone: 250-363-0395
E-mail address: ji-yonisabell.park@pwgsc.gc.ca

The Contracting Authority is responsible for the management of the Contract and any changes to the Contract must be authorized in writing by the Contracting Authority. The Contractor must not perform work in excess of or outside the scope of the Contract based on verbal or written requests or instructions from anybody other than the Contracting Authority.

5.2 Technical Authority
The Technical Authority for the Contract is: TBA

The Technical Authority is the representative of the department or agency for whom the Work is being carried out under the Contract and is responsible for all matters concerning the technical content of the Work under the Contract. Technical matters may be discussed with the Technical Authority; however, the Technical Authority has no authority to authorize changes to the scope of the Work. Changes to the scope of the Work can only be made through a contract amendment issued by the Contracting Authority.

5.3 Contractor's Representative

Name:
Title:
Company:
Address:
Telephone:
Facsimiles:
E-mail address:
Mobile:

5.4 Procurement Authority

The Procurement Authority for the Contract is: TBA

The Procurement Authority is the representative of the department or agency for whom the Work is being carried out under the Contract. The Procurement Authority is responsible for the implementation of tools and processes required for the administration of the Contract. The Contractor may discuss administrative matters identified in the Contract with the Procurement Authority however the Procurement Authority has no authority to authorize changes to the scope of the Work. Changes to the scope of Work can only be made through a contract amendment issued by the Contracting Authority.

6. Proactive Disclosure of Contracts with Former Public Servants (A3025C)

By providing information on its status, with respect to being a former public servant in receipt of a *Public Service Superannuation Act* (PSSA) pension, the Contractor has agreed that this information will be reported on departmental websites as part of the published proactive disclosure reports, in accordance with Contracting Policy Notice: 2012-2 of the Treasury Board Secretariat of Canada.

7. Payment

7.1 Basis of Payment

The Contractor will be paid in accordance with the Basis of Payment in Annex D.

7.2 Limitation of Price

SACC Manual Clause C6000C (2011-05-16), Limitation of Price

7.3 Method of Payment

7.3.1 SACC Manual Clause H1001C (2008-05-12), Multiple Payments

7.4 SACC Manual Clauses

A9117C (2007-11-30), T1204 - Direct Request by Customer Department

8. Invoicing Instructions

1. The Contractor must submit invoices in accordance with the section entitled “Invoice Submission” of the general conditions. Invoices cannot be submitted until all work identified in the invoice is completed.

2. Invoices must be distributed as follows:

   (a) The original and one (1) copy must be forwarded to the address shown on page 1 of the Contract for certification and payment.

   (b) One (1) copy must be forwarded to the Contracting Authority identified under the section entitled “Authorities” of the Contract.

9. Certifications

9.1 Compliance

Compliance with the certifications and related documentation provided by the Contractor in its bid is a condition of the Contract and subject to verification by Canada during the entire contract period. If the Contractor does not comply with any certification, provide the related documentation or if it is determined that any certification made by the Contractor in its bid is untrue, whether made knowingly or unknowingly, Canada has the right, pursuant to the default provision of the Contract, to terminate the Contract for default.

10. Applicable Laws

The Contract must be interpreted and governed, and the relations between the parties determined, by the laws in force in (*to be inserted at contract award*).

11. Priority of Documents

If there is a discrepancy between the wording of any documents that appear on the list, the wording of the document that first appears on the list has priority over the wording of any document that subsequently appears on the list.

(a) the Articles of Agreement;
(b) the supplemental general conditions 4007 (2010-08-16), Canada to Own Intellectual Property Rights in Foreground Information;
(c) the general conditions 2035 (2014-03-01), General Conditions - Higher Complexity - Services;
(d) Annex A, MEX 4 Statement of work;
(e) Annex B, P32S-64M-4GB Statement of work
(f) Annex C, P32S-64M-4GB Product design specification
(g) Annex D, Basis of Payment;
(h) the Contractor's bid dated (insert date of bid) (If the bid was clarified or amended, insert at the time of contract award: "as clarified on _____" ***or*** ", as amended on _____" and insert date(s) of clarification(s) or amendment(s))

12. Insurance

The Contractor is responsible for deciding if insurance coverage is necessary to fulfill its obligation under the Contract and to ensure compliance with any applicable law. Any insurance acquired or maintained by the Contractor is at its own expense and for its own benefit and protection. It does not release the Contractor from or reduce its liability under the Contract.

ATTACHMENT A

MANDATORY TECHNICAL CRITERIA

1. Mandatory Technical Criteria

At bid closing time, the Bidder must comply with the following mandatory technical criteria and provide the necessary documentation to support compliance. Any bid which fails to meet the following mandatory technical criteria will be declared non-responsive. Each criterion should be addressed separately.

1.1 Instructions for completing this section

Your proposal must address each item and be compliant, or your proposal will be deemed non-responsive and no further consideration of the proposal will be given.

If there is insufficient space in the table, assign SIR # (Supplementary Information Reference) and provide the appropriate details on a separate page in your proposal.

NOTE: When no published documentation is currently available, (or applicable), indicate the acronym CSP, (for: "Certified by Signature on our Proposal").

EXAMPLE:

ITEM	SPECIFICATION	M = Mandatory	BIDDER'S RESPONSE	Met (yes/no) & points	Bidders SIR#.
3.1	The box has a range of z-y frequencies	M	*Agreed. Also see our brochure included in bid package.*	*yes*	*For additional details refer to SIR # 01, in our proposal*

SIR# 01 - ITEM:3.2 Since 1988 our company is a manufacturer which produces similar equipment to the BOX specified. We have multiple configurations not typically advertised and can meet your requirements. Please refer to our attached – custom specification build sheet.

Technical Proposal

MEX 4 Project

ITEM	SPECIFICATION	M = Mandatory	BIDDER'S RESPONSE	Met (yes/no)	Bidders SIR#.
1	Demonstrated history of developing, fabricating, and testing high-speed circuit boards with minimum 10 Gbps per pair performance. Provide at least two example projects with references, and describe high-speed circuit board design methods utilized (board material, stackup, copper geometries).	M			

ITEM	SPECIFICATION	M = Mandatory	BIDDER'S RESPONSE	Met (yes/no)	Bidders SIR#.
2	Evidence of recent history of development (or currently in development) of high-speed circuit boards with up to 28 Gbps per pair performance goal. List at least one project and describe high-speed circuit board design methods utilized (board material, stackup, copper geometries); provide example technical drawings as additional supporting evidence.	M			

P32S project
IMPORTANT: Bidders who wish to be considered for the PS32 Project must respond to items 1 and 2 of the MEX4 table and items (1, 2, 3 & 4) per the table below.

ITEM	SPECIFICATION	M = Mandatory	BIDDER'S RESPONSE	Met (yes/no)	Bidders SIR#.
1	Demonstrated history of developing, fabricating, and testing high-speed circuit boards of similar performance, feature sizes, complexity, size, and density to the P32S, with minimum 10 Gbps per pair performance. Provide at least two example projects with references, and describe high-speed circuit board design methods and approaches utilized (board material, stackup, copper geometries).	M			
2	Evidence of recent history of development (or currently in development) of high-speed circuit boards of similar performance, feature sizes, complexity, size, and density to the P32S, with at least 28 Gbps per pair performance goal. List at least one project and describe high-speed circuit board design methods utilized (board material, stackup, copper geometries); provide example technical drawings as additional supporting evidence.	M			
3	Describe manufacturing process and tests envisioned to ensure Reliability, Product Assurance, and Quality Assurance according to sections 10. and 11. of the PowerMX Base Specification.	M			

ITEM	SPECIFICATION	M = Mandatory	BIDDER'S RESPONSE	Met (yes/no)	Bidders SIR#.
4	Developer must meet Product Assurance mandatory requirements defined in section 11.2 of the PowerMX Base Specification. Provide documentation evidence of compliance.	M			

Note 1. NRC will provide supplier with desired layer stack up and via strategies as well as provide support as and when requested to run HyperLynx Signal Integrity checks on supplier's PCB designs.

Note 2**.** NRC recognizes that there is technical risk in the execution of the contract(s) with no guarantee of success. Therefore, NRC expects the Contractor will proceed on a **best effort basis** to meet requirements stated in the SOWs and evaluation of the contract deliverables will be evaluated accordingly.

MEX4

4-site PowerMX Mechanical/Electrical Model

STATEMENT OF WORK

Version: *1.2*

Date: *April 14, 2014*

Author: *Brent Carlson*

Document History

Version	Date	Changes/Notes	Author
DRAFT	2014-01-07	First draft release for internal review.	B. Carlson
1.0	2014-01-10	Initial version for quotation.	B. Carlson
1.1	2014-01-24	Add J9 and J10 on the motherboard for test set calibration. Release for PWGSC tendering cycle.	B. Carlson
1.2	2014-04-14	Provide web reference for the Base Specification, www.powermx.org. Remove vendor's requirement for post-layout simulation/performance verification (NRC will do this).	B. Carlson

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Definitions, Acronyms, and Abbreviations

For most definitions and acronyms, refer to the PowerMX Base Specification [1].

Others are as follows:

MEX4 – Generic name for this multi-board design/build project.

MEX4-MB – Specifically, the motherboard of this project.

MEX4-IOB – Specifically, the I/O board of this project.

MEX4-PMXM – Specifically, the mezzanine PMXM board of this project.

SOW – Statement of Work.

PCB – Printed Circuit Board.

SMA – "Sub-miniature version A" coaxial connectors.

GND – Ground.

NRC – National Research Council.

BGA – Ball Grid Array.

1 Introduction & Scope

This document defines the Statement of Work (SOW) for the "MEX4" PowerMX mechanical/electrical model project.

A serious user of this document must fully read and understand relevant sections of the PowerMX Base Specification [1] **in order to understand the scope and effort required to execute this SOW.** This SOW document, in conjunction with the PowerMX Base Specification (hereafter referred to at the "Base Specification"), fully defines the scope of the "MEX4" project including product definition, tasks, deliverables, and build quantities.

The purpose of the MEX4 project is to fabricate representative physical models, containing electrical test coupons, of the PowerMX 4-site motherboard, PMXM module, and monolithic PMX_IOC. Each of these is to be fabricated according to the Base Specification, as further described in the next section on Product Build Descriptions.

There are 3 PCB/assembly builds in this project:

1. **MEX4-MB** – 4-site PowerMX motherboard.
2. **MEX4-IOB**—monolithic PMX_IOC plug in module.
3. **MEX4-PMXM**—PMXM plug in mezzanine card.

Where not explicitly stated, figure and section references in this SOW refer to figures and sections in the Base Specification.

2 Product Build Descriptions

This section contains descriptions of PCB assemblies that are to be fabricated within the scope of this SOW. Note that these builds will not have power applied, or contain power supplies of any kind.

2.1 MEX4 Motherboard (MEX4-MB)

2.1.1 MEX4-MB Overview

The MEX4 project motherboard—named **"MEX4-MB"**—requirements are as follows:

1. Full 4-site motherboard according to the Base Specification, Figure 5-1 and 5-2 (PCB thickness), including Area-1, Area-2, and Area-3 connectors as specified, as well as:
    a. PMX_IOC connectors, pads, and holes, according to Figure 5-3 (and associated detail Figures 5-4, 5-5), at all 8 PMX_IOC instances/sites.
    b. PMXM connectors, pads, and holes, according to Figure 5-6 in all 4 Sites, including the MCA connector as well as V1-V4, and VC power sockets as per Figure 5-6, *Note 1*. VCep pins are not required.
2. For Area-1, place two right-angle PCB-mount SMA connectors as indicated, and further defined in Figure 5-7.
3. For Area-2, exactly according to Figure 5-1, and further defined in Figure 5-8(a).
4. For Area-3, exactly according to Figure 5-1 (ATX V2.2 connector, section 5.5.2(3.)).
5. RJ-45 right-angle, PCB-mount connector, as shown in Figure 5-1, Front Side. P/N is designer's choice.
6. 28-layer PCB material, stackup, and traces according to section 2.1.2 of this document.
7. On the **Front Side**, in the area to the right of Site 1 PMXM site, 8 straight PCB-mount SMA jack connectors (Molex P/N: 73251-1850, or equivalent), J1-J8 Figure 2-1. Each one routes single-ended, 50 ohm stripline to a surface mount coaxial pad in each PMX_IOC site APMX connector, coordinate (12.5,28.5) of Figure 5-4 of the Base Specification. See section 2.1.4 of this document for further PCB information.

2.1.2 MEX4-MB PCB Stackup

NRC will provide more specific via and pad geometry information as an Annex document/instructions to this SOW, once this information becomes available from investigations currently in progress.

1. 28 layers, 1/2 oz per layer (TBC).
2. Front Side to Rear Side stackup: GND(1)-sig(2)-GND(3)-sig(4),…,sig(14)-sig(15)-GND(16)-sig(17), …, GND(28).
3. Finished thickness as per Base Specification, Figure 5-2 (i.e. 3.175 mm +/-0.1mm).
4. Use Megatron-6 material (layers 1-14; layers 15-28 contain no active traces and could be built of cheaper material provided mechanical balance/integrity is achieved) build in two 14-layer mirror-identical halves, laminate and plate thru (if required) for final 28 layers.

2.1.3 MEX4-MB PCB layout

The full MEX4 Front Side motherboard component layout, with all PMXM and PMX_IOC sites populated is shown in Figure 2-1.

1. **J1-J4** are surface press-mount test SMA coaxial connectors for connecting single-end 50 ohm stripline traces to PMX_IOC 1-B to 4-B APMX surface mount coaxial pads. J5-J8 perform the same function for PMX_IOC 1-A to 4-A APMX coaxial pads. **J9** and **J10** are for test header and test set cable calibration.

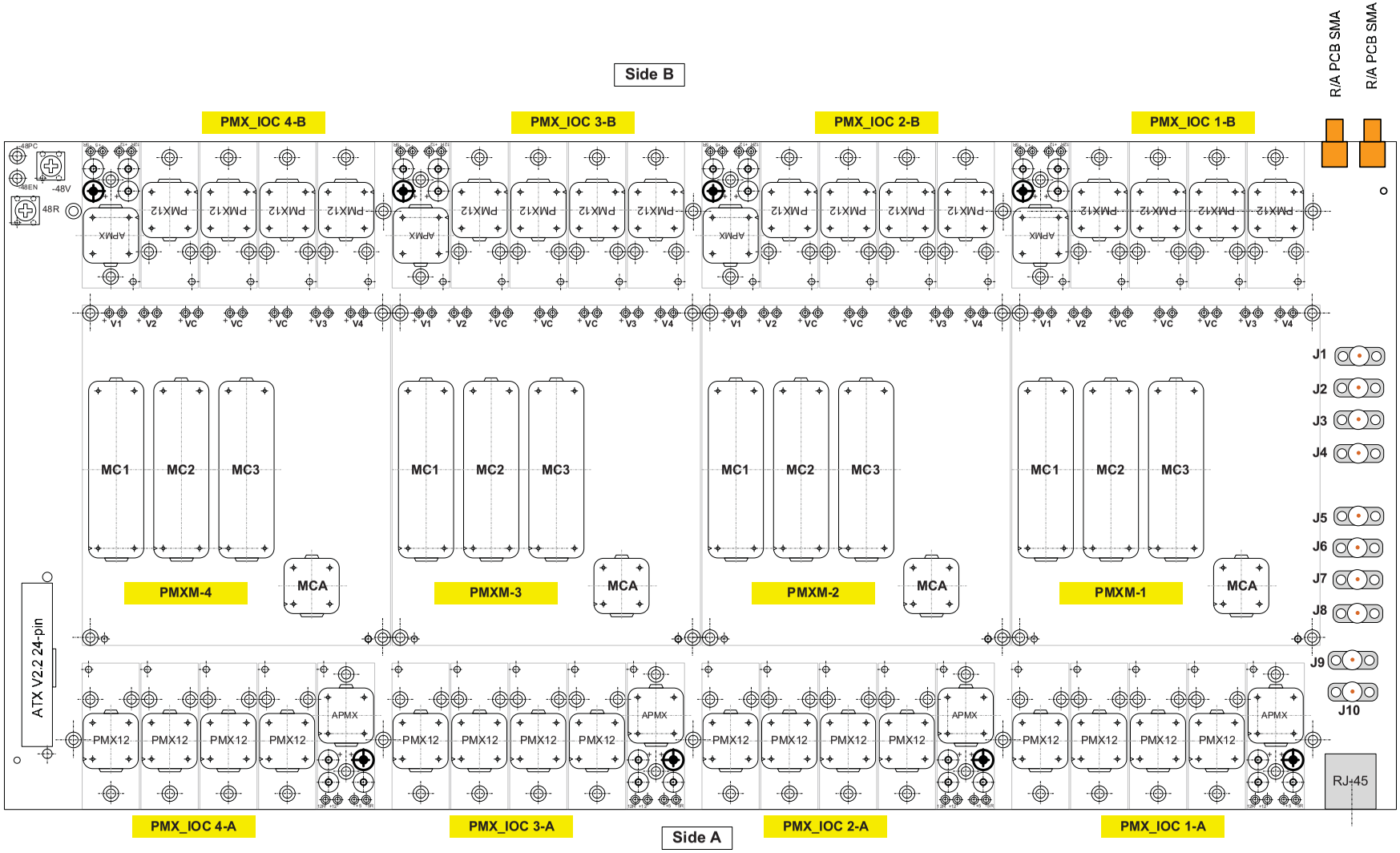

Figure 2-1 MEX4-MB Front Side layout. There are no Rear Side components.

2.1.4 MEX4-MB PCB schematic and routing

NRC will provide more specific via and pad geometry information as an Annex document/instructions to this SOW, in the interim, however, the current baseline concept is shown in Figure 2-2. Multi-layer vias, anti-pads, and back drilling are anticipated, but no microvias are required. Only layers 1-14 contain ground and routing traces.

The schematics for the motherboard must be developed according to the following instructions, noting that only a few connections (compared to the full Base Specification) are established for differential pair and single-ended transmission line performance testing and verification.

1. All Meg-Array connectors (MC1-3, MCA, PMX12, APMX) which have grounded pins according to the Base Specification, are connected/soldered to layer 1 GND plane thermal-relief BGA pads. All other Meg-Array connections, unless otherwise noted in this section, are soldered to unconnected layer 1 BGA pads.
2. All other connectors' (power studs, Area-1 SMA, RJ-45, ATX) pins/pads in the Base Specification that are not ground are soldered (or press-fit for power studs) to unconnected pads.
3. Layer 1-14 GND stitching vias on both sides of differential pairs and single-ended lines, with 0.100" (TBC) spacing.
4. Layer 1-14 GND stitching vias within all Meg-Array BGA arrays.
5. Route **J1-J4** and **J5-J8** 50 ohm coaxial connectors, stripline connections with surrounding GND stitching vias, **on layers 2 and 4** according to Table 2-1:

   Table 2-1 J1-J4 and J5-J8 connections to PMX_IOC surface-mount coaxial pads.

Coaxial Connector	Connects to PMX_IOC APMX:
J1	1-B
J2	2-B
J3	3-B
J4	4-B
J5	4-A
J6	3-A
J7	2-A
J8	1-A

   Note that the APMX coaxial connectors to which the above routing occurs are **highlighted bold** in Figure 2-1. These single-ended connections will be tested to 5 GHz.

6. Establish the following differential pair connections for all PMXM sites to companion PMX_IOC sites, according to Table 6-6 and 6-7 of the Base Specification:
   a. MC3: AL1[0]+/- (MC3 pins C4,D4, routes to PMX_IOC/PMX12 Side A P1 pins B2,C2).
   b. MC3: AL1[1]+/- (MC3 pins C6,D6, routes to PMX_IOC/PMX12 Side A P1 pins B4,C4).
   c. MC3: AL1[2]+/- (MC3 pins C8,D8, routes to PMX_IOC/PMX12 Side A P1 pins B6,C6)
   d. MC1: BL1[0]-/+ (MC1 pins AQ8,AR8, routes to PMX_IOC/PMX12 Side B P1 pins C2,B2).
   e. MC1: BL1[1]-/+ (MC1 pins AQ6,AR6, routes to PMX_IOC/PMX12 Side B P1 pins C4,B4).

f. MC1: BL1[2]-/+ (MC1 pins AQ4,AR4, routes to PMX_IOC/PMX12 Side B P1 pins C6,B6).

Route a., b., and c. on layer 6, with minimum-spec pair-to-pair separation TBD in companion Annex document. Route d., e., and f. on layer 12 in a similar manner.

7. Establish the following differential pair connections for all PMXM-to-PMXM nearest-neighbour sites, according to Table 6-6 of the Base Specification:
   a. MC1: LL1[0]+/- (i.e. MC1 pins G4,H4 to left-neighbour MC3 pins G10,H10).
   b. MC1: LL1[1]+/- (i.e. MC1 pins G2,H2 to left-neighbour MC3 pins G8,H8).
   c. MC1: LL1[2]+/- (i.e. MC1 pins J9,K9 to left-neighbour MC3 pins J3,K3)
   d. MC3: RL1[0]+/- (i.e. MC3 pins G10,H10, to right-neighbour MC1 pins G4,H4).
   e. MC3: RL1[1]+/- (i.e. MC3 pins G8,H8, to right-neighbour MC1 pins G2,H2).
   f. MC3: RL1[2]+/- (i.e. MC3 pins J3,K3 to right-neighbour MC1 pins J9,K9)

   Where a PMXM connector has no nearest neighbour (i.e. Site 1—Right, Site 4—Left) leave the particular pairs unconnected. Route all differential pairs on layer 6, at minimum specified pair-to-pair separation. This allows for channel-to-channel cross-talk tests.
8. **J9** connects directly to **J10**, 50 ohm microstrip, via the shortest route possible. These connectors and this connection are required for test set and connector calibration.

A baseline MC1-MC3 Meg-Array via breakout and routing concept is shown in Figure 2-2. Note that the diagram shows anti-pads overlapping causing breaks in ground plane coverage, something that cannot occur and a side-effect of lack of dimensional precision in the drawing. Since high-performance (minimum 20 Gbps per pair) is required, via back-drilling is necessary to avoid stubs.

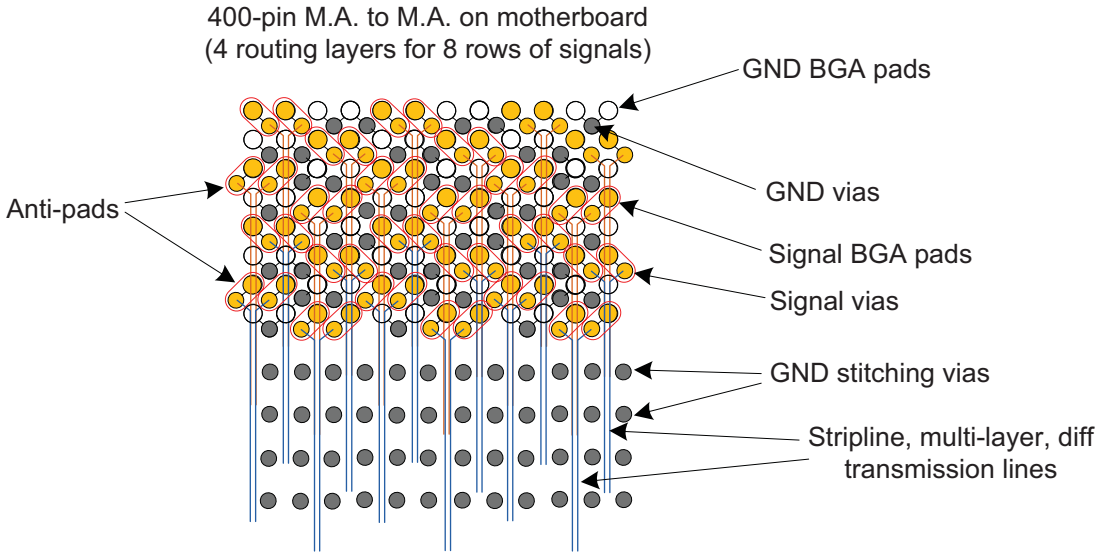

Figure 2-2 MC1-3 Meg-Array via breakout concept.

2.2 MEX4 PMX_IOC Plug-in Module (MEX4-IOB)

2.2.1 MEX4-IOB Overview

The MEX4 project PMX_IOC plug-in module requirements are as follows:

1. Monolithic plug-in module according to section 5.6 (Figure 5-10, and associated figures) of the Base Specification, including all connectors, pads, power pins, locator pins (only two are installed, Base Specification section 5.6.1 clause(4.)), and all four surface-mount coaxial connectors as stated. Figure 5-10 "*Note 1*" dimension set to 25 mm +/- 1 mm. This module mates with PMX_IOC sites in the MEX4-MB motherboard.
2. Use PCB thickness for this plug-in module of 0.125" +/- 0.010". The PCB thickness is not specified in the Base Specification.
3. 7 straight PCB-mount SMA jack connectors (Molex P/N: 73251-1850, or equivalent), mounted in the free area (between coordinate 0.0 and *Note 1* dimension of Figure 5-10) on the **Front Side** of the test PMX_IOC plug-in module, according to 2.2.3 of this document. Six of these route 6 single-ended stripline traces to the P1 PMX12 FCI 100-pin Meg-Array connector; 1 routes 1 single-ended stripline trace to 1 APMX coaxial connector (coordinate (12.5,28.5), Figure 5-11 of the Base Specification).

2.2.2 MEX4-IOB PCB Stackup

NRC will provide more specific via and pad geometry information as an Annex document/instructions to this SOW.

1. 28 layers, 1/2 oz per layer (TBC).
2. Front Side to Rear Side stackup: GND(1)-sig(2)-GND(3)-sig(4),…,sig(14)-sig(15)-GND(16)-sig(17), …, GND(28).
3. Finished thickness 0.125" +/- 0.010".
4. Use Megatron-6 material built in two 14-layer mirror-identical halves, laminate and plate thru (as required) for final 28 layers.

2.2.3 MEX4-IOB Layout

The plug-in module layout consists of the through-holes, connectors, pads, and pins on the Rear Side according to Figure 5-10 of the Base Specification, as well as 7 straight PCB-mount SMA jack connectors (Molex P/N: 73251-1850, or equivalent) mounted on the Front Side. The *Front Side* layout, "looking through" to the Rear Side connectors is shown in Figure 2-3:

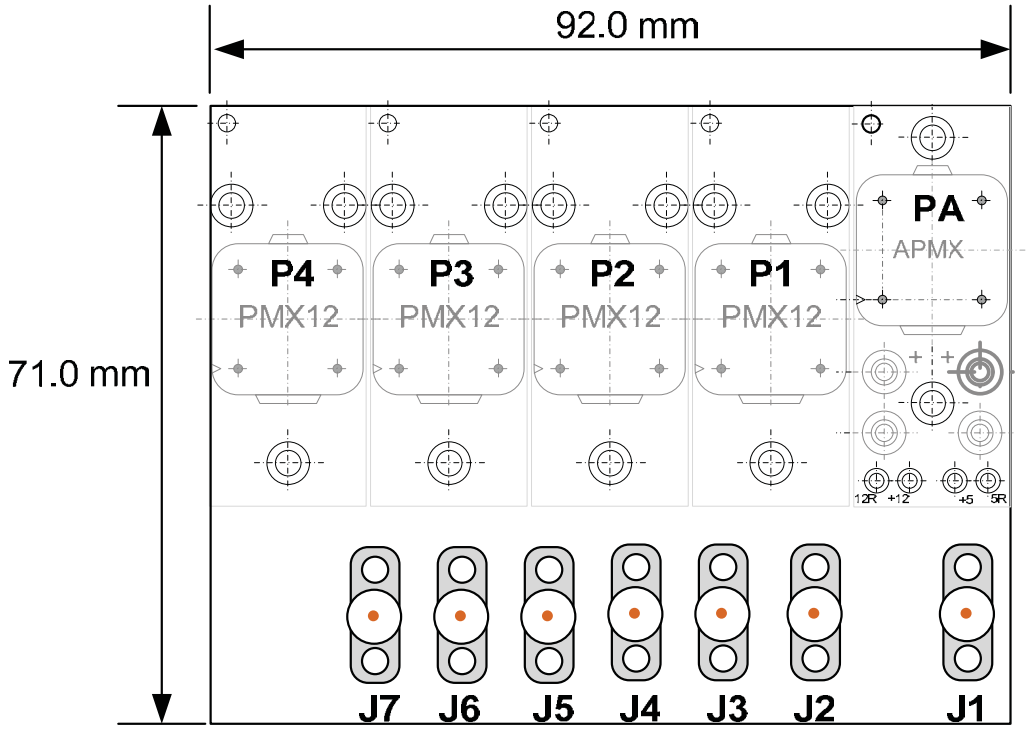

Figure 2-3 MEX4-IOB PCB Front Side layout looking through to the Rear Side. Meg-Array, pins, and surface-mount Tyco pressure-contact coaxial connectors are mounted on the Rear Side. SMA test jack connectors (J1-J7) are mounted on the Front Side.

2.2.4 MEX4-IOB PCB schematic and routing

NRC will provide more specific via and pad geometry information as an Annex document/instructions to this SOW. Multi-layer vias, anti-pads, and back drilling are anticipated to facilitate performance exploration, but no microvias are required.

The schematics for the MEX4-IOB must be developed according to the following instructions, noting that only a few connections (compared to the full Base Specification) are established for differential pair and single-ended transmission line performance testing and verification.

1. All Meg-Array connectors (PA, P1-P4) which have grounded pins according to the Base Specification (APMX Table 6-2, PMX12 Table 6-4), are connected/soldered to layer 1 GND plane thermal-relief BGA pads. All other Meg-Array connections, unless otherwise noted in this section, are soldered to unconnected layer 1 BGA pads.
2. All other connectors' pins/pads, unless otherwise noted in this section, that are not ground (in the Base Specification) are soldered to unconnected pads.
3. Layer 1-28 GND stitching vias on both sides of (differential pairs, if applicable and) single-ended lines, with 0.100" (TBC) spacing.

4. Layer 1-28 GND stitching vias within all Meg-Array BGA arrays.
5. Route **J1** single-ended 50 ohm stripline on layer 2, to the surface mount Tyco coaxial connector within the APMX footprint highlighted in bold in Figure 2-3.
6. Route J2-7 to P1 Meg-Array pins according to Table 2-2. These should be individual 50-ohm single-ended stripline traces since they are routing to individual SMA connectors.

Table 2-2 MEX4-IOB test SMA connector routing.

Coaxial Connector	P1 pin
J2	B2
J3	C2
J4	B4
J5	C4
J6	B6
J7	C6

2.3 MEX4 PMXM Mezzanine Card (MEX4-PMXM)

2.3.1 MEX4-PMXM Overview

The MEX4-PMXM mezzanine card requirements are as follows:

1. Mezzanine card according to section 5.7, Figure 5-13 of the Base Specification. Includes all connectors, pads, holes, and pins (V1-V4, VC) indicated in the figure.
2. Use PCB thickness for this plug-in module of 0.125" +/-0.010". The PCB thickness is not specified in the Base Specification.
3. 24 straight PCB-mount SMA jack connectors (Molex P/N: 73251-1850, or equivalent), mounted on the **Front Side** of the PMXM module, according to section 2.3.3 of this document. Six of these route 6 single-ended/differential[1] signals through MC3 to PMX_IOC P1 (Side A); in a similar way, 6 of these route 6 single-ended/differential signals through MC1 to PMX_IOC P1 (Side B). 6 of these route to the Left nearest-neighbour PMXM via MC1, and the last 6 route to the Right nearest-neighbour PMXM via MC3.

2.3.2 MEX4-PMXM PCB Stackup

NRC will provide more specific via and pad geometry information as an Annex document/instructions to this SOW.

5. 28 layers, 1/2 oz per layer (TBC).
6. Front Side to Rear Side stackup: sig(1)-GND(2)-sig(3)-GND(4), …, sig(13)-GND(14)-GND(15)-sig(16), …, GND(27)-sig(28).
7. Finished thickness 0.125" +/-0.010".

[1] As will be shown, differential on the Rear Side layers, and single-ended on the Front Side layers.

8. Use Megatron-6 material build in two 14-layer mirror-identical halves, laminate and plate thru (as required) for final 28 layers.

2.3.3 MEX4-PMXM Layout

The MEX4-PMXM module layout consists of the through-holes, connectors, pads, and pins on the Rear Side according to Figure 5-13 of the Base Specification, as well as 24 straight PCB-mount SMA jack connectors (Molex P/N: 73251-1850, or equivalent) mounted on the Front Side. The *Front Side* layout, "looking through" to the Rear Side connectors is shown in Figure 2-4.

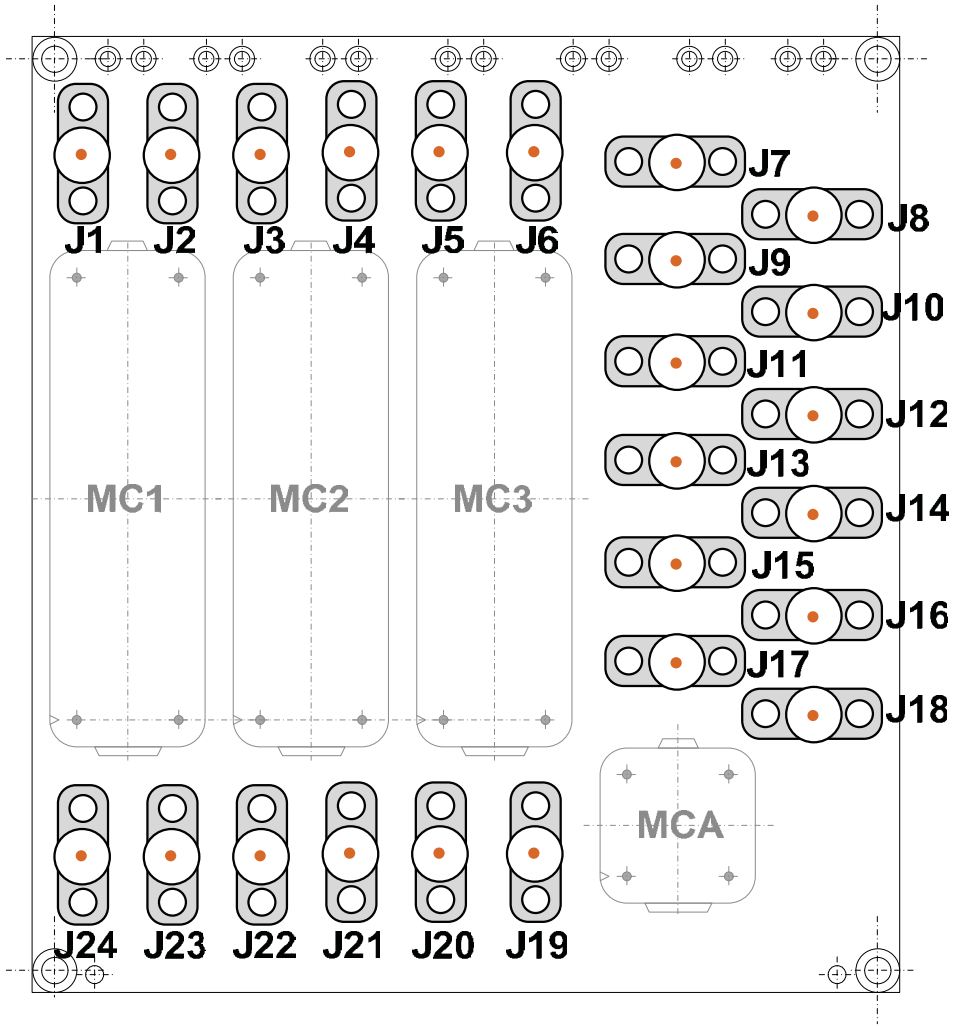

Figure 2-4 MEX4-PMXM layout, Front Side looking through to MC1-3 and MCA Meg-Array connectors located on the Rear Side.

2.3.4 MEX4-PMXM PCB schematic and routing

NRC will provide more specific via and pad geometry information as an Annex document/instructions to this SOW, however, in the interim, an example of the anticipated Rear Side via breakout and routing is

shown in Figure 2-5. Multi-layer vias, anti-pads, back drilling, L1-2, 1-3 microvias, and L28-27, 28-26 microvias are anticipated to facilitate performance exploration.

The schematics for the MEX4-PMXM must be developed according to the following instructions, noting that only a few connections (compared to the full Base Specification) are established to SMA test headers for single-ended transmission line performance testing and verification.

1. All Meg-Array connectors (MC1-3, MCA) which have grounded pins according to the Base Specification (section 6.6.2.3 clause (30.)), are connected/soldered to layer 27 GND plane BGA microvia-in-pads. All other Meg-Array connections, unless otherwise noted in this section, are soldered to unconnected layer 28 BGA pads.
2. Layer 1-28 GND stitching vias on both sides of (differential pairs, if applicable and) single-ended lines, with 0.100" (TBC) spacing.
3. Layer 27-25 GND stitching vias within all Meg-Array BGA arrays on a regular grid (not shown in Figure 2-5), as closely packed as possible. This likely requires alternation of microvia/breakout patterns shown in the figure. These could feed-thru to layer 15, but as they are on a 1.27 mm grid, must not contact/overlay 1 mm grid[2] vias on layers 1-14.

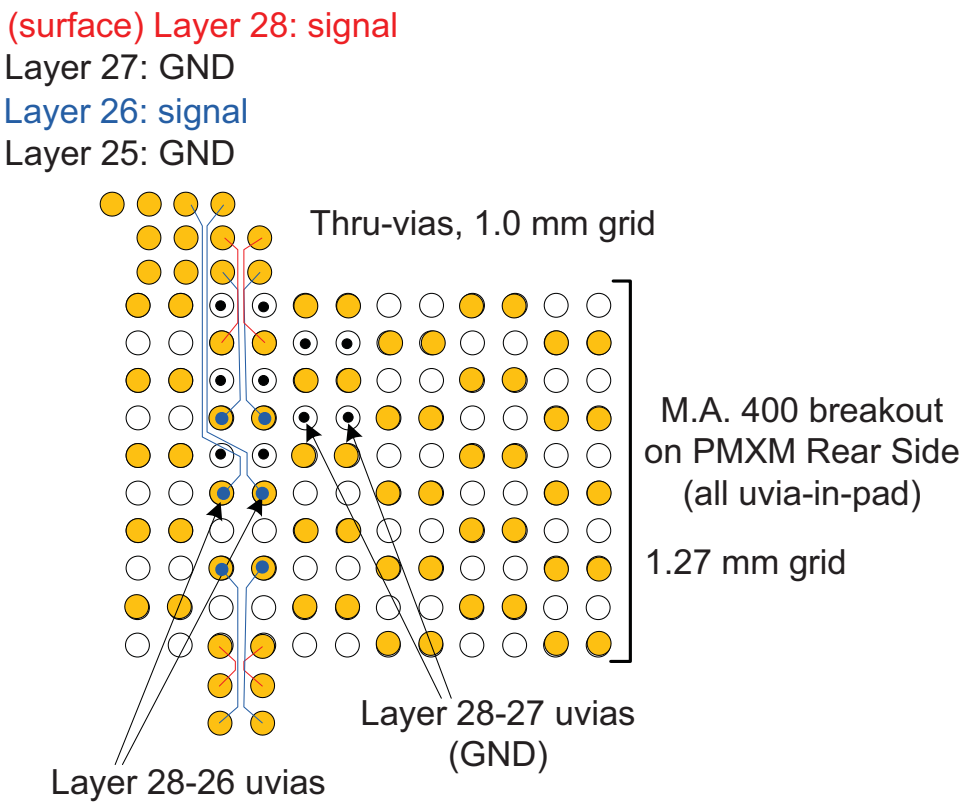

Figure 2-5 Example anticipated Rear Side via breakout and routing.

[2] So as to accommodate Front Side FPGAs, although such FPGAs are not part of this build.

4. Route J1-24 to MC1-MC3 Meg-Array pins according to Table 2-3. These should be individual 50-ohm single-ended stripline traces since they are routing to individual SMA connectors. The table notes which nearest-neighbour PMXM (Right and Left) as well as MEX4-IOB SMA test headers each of J1-24 connects to.

Table 2-3 MEX4-PMXM test SMA header routing.

Coaxial Connector	Meg-Array Pin	Signal (IOC coax hdr)	Notes
J1	MC1-AQ4	BL1[2]- (IOC J7)	Connects to Side B MEX4-IOB SMA test headers
J2	MC1-AR4	BL1[2]+ (IOC J6)	
J3	MC1-AR6	BL1[1]+ (IOC J4)	
J4	MC1-AQ6	BL1[1]- (IOC J5)	
J5	MC1-AR8	BL1[0]+ (IOC J2)	
J6	MC1-AQ8	BL1[0]- (IOC J3)	
J7	MC3-K3	RL1[2]-	Connects to Right PMXM J13-14
J8	MC3-J3	RL1[2]+	
J9	MC3-H8	RL1[1]-	Connects to Right PMXM J15-16
J10	MC3-G8	RL1[1]+	
J11	MC3-H10	RL1[0]-	Connects to Right PMXM J17-18
J12	MC3-G10	RL1[0]+	
J13	MC1-K9	LL1[2]-	Connects to Left PMXM J7-8
J14	MC1-J9	LL1[2]+	
J15	MC1-H2	LL1[1]-	Connects to Left PMXM J9-10
J16	MC1-G2	LL1[1]+	
J17	MC1-H4	LL1[0]-	Connects to Left PMXM J11-12
J18	MC1-G4	LL1[0]+	
J19	MC3-C8	AL1[2]+ (IOC J6)	Connects to Side A MEX4-IOB SMA test headers
J20	MC3-D8	AL1[2]- (IOC J7)	
J21	MC3-C6	AL1[1]+ (IOC J4)	
J22	MC3-D6	AL1[1]- (IOC J5)	
J23	MC3-C4	AL1[0]+ (IOC J2)	
J24	MC3-D4	AL1[0]- (IOC J3)	

3 Tasks & Deliverables

3.1 Tasks

The task list for this project is as follows:

1. Review this SOW and clarify details with NRC as necessary.
2. Build the schematics for each of the boards (MEX4-MB, MEX4-IOB, MEX4-PMXM). Review schematics with NRC to ensure correctness.
3. Layout and route each of the boards as defined in section 2. As previously mentioned, further, more detailed via and trace routing and stackup information will be provided by NRC, but it is up to the supplier to ensure board stackup, via geometry, and routing meets impedance requirements (50 ohm single-ended; 100 ohm differential) for achieving minimum 20 Gbps performance[3]. The supplier must provide a generic post-layout format (e.g. Gerber or ODB – TBC) that NRC can use for post-layout performance verification. Front and/or Rear Side silkscreen layers must be added as appropriate to identify connectors in the Base Specification, and test SMA connectors (i.e. J*) in this SOW.
4. Once NRC approves the layout, fabricate, populate[4], and deliver the following board quantities:
    a. MEX4-MB – Qty = 1.
    b. MEX4-IOB – Qty = 8.
    c. MEX4-PMXM – Qty = 4.

    The supplier is responsible for all component procurement and manufacturing processes. Standard bare-PCB testing, and only post component reflow X-ray testing is required. Power will never be applied to this board.
5. Deliver to NRC the stated quantities.

3.2 Deliverables

1. Schematics for all 3 boards for NRC approval. These must be in .pdf drawing format.
2. Layout and routing diagrams for all 3 boards for NRC approval. These could be in Gerber format or pdf drawing printouts.
3. Post-layout files for NRC post-layout verification (as noted in bullet 3. of section 3.1) of high speed single-ended and differential traces connecting to SMA coaxial test headers.
4. Populated and built boards in quantities noted, ready for NRC card mating and actual signal performance testing.
5. All associated design artefacts including schematics, BOM, assembly, and mechanical drawings (if any).

[3] MEX4-MB J1-J8 to MEX4-IOB J1 connections will be tested up to 5 GHz.
[4] Including installation of the test SMA connectors.

4 References

[1] PowerMX Base Specification, Version: Preliminary. See: http://www.powermx.org

5 Appendix

For information purposes, a 3D representation of the MEX4-MB motherboard, with a single MEX4-PMXM plug-in board and MEX4-IOB plug-in board (but with the Note 1 dimension of Figure 5-10 of the Base Specification set to 0), is shown in Figure 5-1. Note that no test SMA connectors are shown.

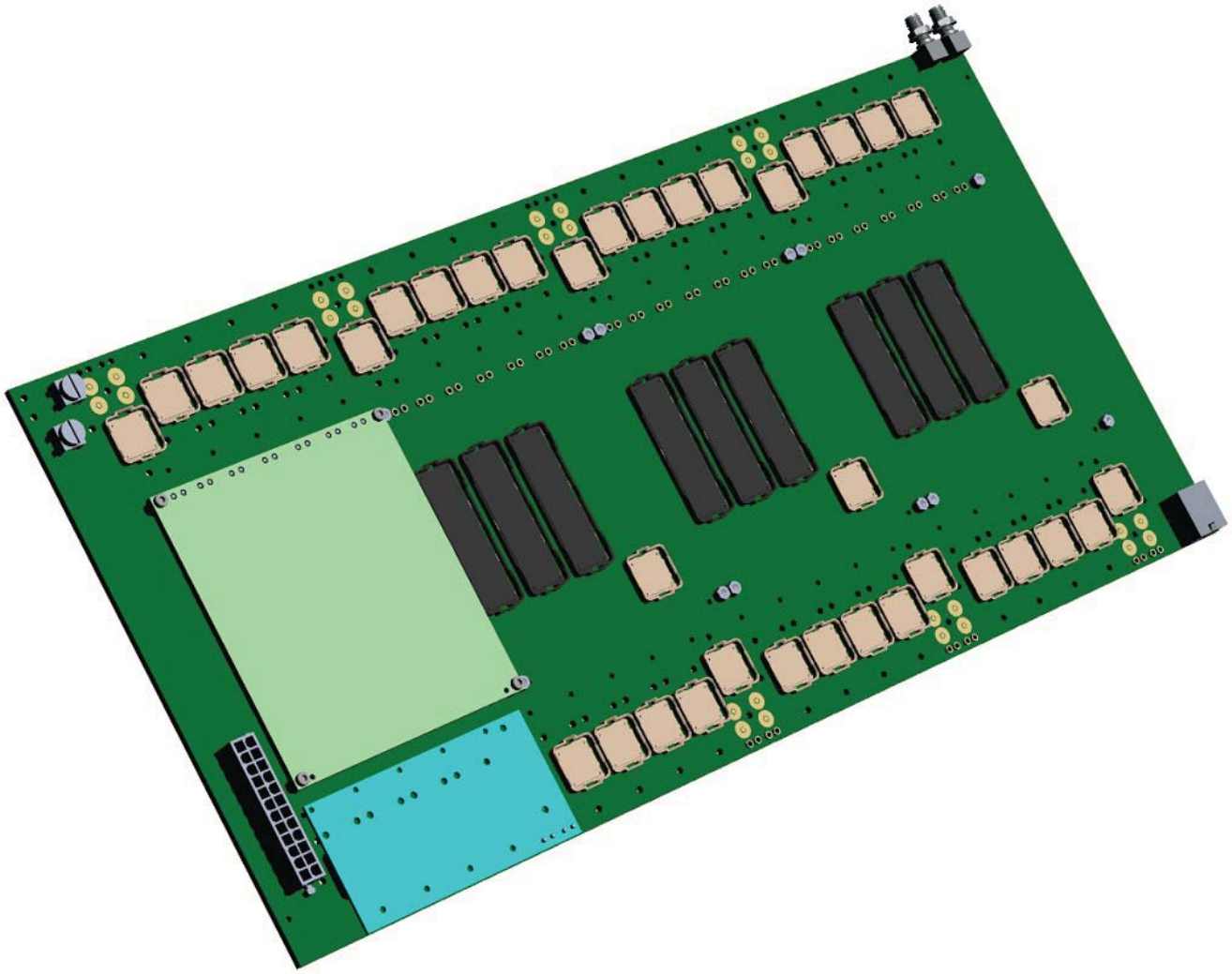

Figure 5-1 3D model of MEX4-MB, MEX4-PMXM, and (shortened) MEX4-IOB. No test SMA connectors are shown.

P32S-64M-4GB

Altera Arria/Stratix-10 FPGA PMXM Module

STATEMENT OF WORK

Version: *1.1*

Date: *April 14, 2014*

Author: *Brent Carlson*

Document History

Version	Date	Changes/Notes	Author
1.0	2014-02-04	Initial release for budgetary quotation and purchase requisition process.	B. Carlson
1.0	2014-02-10	Add Base Specification QA testing to Phase 2.	B. Carlson
1.1	2014-04-14	Include only schematic, layout, routing, and cost analysis in this SOW.	B. Carlson

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Definitions, Acronyms, and Abbreviations

For most definitions and acronyms, refer to the PowerMX Base Specification [1] and the Product Design Specification [2].

BOM – Bill of Materials.

DFM – Design for Manufacturing.

DFT – Design for Test.

DRC – Design Rule Check.

PO – Purchase Order.

RFQ – Request for Quote.

1 Introduction

This document defines the Statement of Work (SOW) for the "P32S-64M-4GB" (hereafter abbreviated "**P32S**" for succinctness) PowerMX PMXM mezzanine/plug-in module project. Refer to the P32S Product Design Specification [2] for detailed requirements and design information.

A serious user of this document must fully read and understand the P32SProduct Design Specification in order to understand the scope and effort required to execute this SOW.

There is only one major phase within this SOW, defined as follows:

- PCB design, layout, routing, and cost analysis of the P32S. This includes progressing the hardware design complete to the point of being ready for prototype fabrication, as well as performing prototype and production cost analysis. NRC will provide PCB material, stackup, and trace/via geometry information (for high-speed SERDES channels) required to successfully design the board. NRC will perform post-layout signal integrity analysis of SERDES channels and all other traces to verify performance prior to prototype fabrication.

Note that the execution of this SOW is for NRC to fully pay for engineering and test services, and fully own the design thereafter, including all schematics, layout source files, and any other associated information.

2 Tasks & Deliverables

This section defines tasks and deliverables for this SOW.

2.1 Tasks

1. Analyze the design using the Product Design Specification [2], Base Specification [1], and PCB material, stackup, and via/trace information as inputs. Iterate with NRC to ensure the requirements of the design are understood and sufficiently defined. Update the Product Design Specification to reflect any changes as necessary.
2. Develop schedule and budget for Phase 1 work. Generate monthly progress reports to NRC against this schedule and budget.
3. Develop schematics, review these and the layout and routing strategy with NRC, and obtain NRC's approval, before proceeding further.
4. Develop preliminary Qty=10, Qty=100, Qty=1000 turnkey cost analysis report, delivered to NRC.
5. Layout and route the board to completion:
    a. Iterate with NRC regarding PCB stackup, material, and component choices as necessary, to meet the Product Design Specification.
    b. Perform all PCB DRCs, and manufacturing DFM and DFT analysis.
    c. Write report describing the design.
    d. Deliver schematics and PCB design files to NRC for analysis and post-layout simulation verification.

e. Develop prototype assembly notes, BOMs, and assembly drawings, ready for prototype fabrication.

At the end of this activity, the design and documentation is ready for prototype fabrication.

2.2 Deliverables

1. Updated Product Design Specification and SOW as required, signed off by NRC. This is a plan of what is to be built before work starts.
2. Schedule and budget. Monthly progress report against this schedule and budget.
3. Schematics and layout/routing strategy reviewed with NRC before proceeding to layout and routing.
4. Qty=10, Qty=100, Qty=1000 turnkey cost analysis report.
5. Post-layout and routing information in format TBD for NRC to use in post-layout signal integrity analysis.
6. PCB DRC report.
7. PCB build DFM report.
8. PCB build DFT report.
9. P32S schematics, PCB design/build files, assembly notes, BOMs, assembly drawings, and any other pertinent “manufacturing package” files.

3 References

[1] PowerMX Base Specification, Version: Preliminary. See: http://www.powermx.org

[2] P32S-64M-4GB Product Design Specification, Version: 1.1, 2014-04-14.

P32S-64M-4GB

PowerMX PMXM Module

Product Design Specification

Version: *1.1*

Date: *April 14, 2014*

Author: *Brent Carlson*

National Research Council Canada
Conseil national de recherches Canada
Canada

Document History

Version	Date	Changes/Notes	Author
1.0	2014-02-04	Initial full release.	B. Carlson
1.1	2014-04-14	Provide web URL reference for Base Specification. Remove requirement for mounting holes for COTS fan heatsink.	B. Carlson

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Definitions, Acronyms, and Abbreviations

For most definitions and acronyms, refer to the PowerMX Base Specification [1].

CDR – Clock Data Recovery; i.e. recovering the receive clock from the (serial) data stream.

EEPROM – Electrically Erasable Programmable Read Only Memory.

JTAG – Joint Test Action Group. Standard signalling for PCB connectivity testing, as well as programming of on-board devices such as EEPROMs. Also used for in-system supervisory communications with various devices.

LVDC – Low Voltage DC.

LVDS – Low Voltage Differential Signalling.

M&C – Monitor and Control.

P/N – Part number.

SGMII – Serial Gigabit Media Independent Interface.

S/N – Serial number.

TBC – To Be Confirmed.

TBD – To Be Defined.

1 Introduction

This document contains key product design and requirements specifications for the "P32S-64M-4GB", a PowerMX PMXM plug-in board with a 96 SERDES channel Altera Arria GX FPGA (footprint compatible and migratable to Arria GT and Stratix-10), and a 4-link, 4GB (or 2GB) HMC memory device. It heavily references the PowerMX Base Specification [1]. Any serious user of this document should fully read and understand the Base Specification to form a complete picture of the product.

This is a working document and a starting point for further detailed design. It has fleshed out the design as much as is possible; further detailed design work builds on this specification, leading to fabricated prototypes, and pre-production prototype units.

2 Product Overview

The P32S-64M-4GB is a PowerMX PMXM plug-in module containing a 96 SERDES channel FPGA, a 4-link, 4GB Hybrid Memory Cube chip, and surrounding support circuitry. Key features of the module are as follows:

1. Altera Arria 10AX900U1F45E2SG FPGA (standard device[1]). This FPGA contains 900 kLEs, 3036 18x19 multipliers, 48 Mbits of on-chip block RAM (M20K SRAM) and 96 17.4 Gbps SERDES transceivers. It is fabricated in 20 nm CMOS in a 45x45 mm 1932 pin BGA package, and is footprint/migration compatible with the GX1150, GT900[2], and GT1150 Arria devices, as well as a Stratix-10 14 nm FinFET device.
2. 4-link 4 GByte Micron HMC dynamic memory chip (MT43A4G80100NFH-S15:A). This device is in a 31 mm BGA package, connects to the Arria FPGA via 64 15G SERDES transceivers, providing 160 Gbytes/sec of raw aggregate memory bandwidth to the FPGA, with ultimate capability of 240 Gbytes/sec[3].
3. 32 SERDES inputs from Side A P1-P4, and 32 SERDES outputs to Side B P4-P1, allowing multiple motherboards to be concatenated with motherboard-to-motherboard PCB/bridging boards. 16 SERDES ("LR" in Figure 2-1) of each of these are footprint compatible with GT 28 Gbps transceivers so as to allow for a higher I/O performance upgrade path.
4. 8 Gbit (512k x 16) DDR3L memory chip (Micron MT41K512M16-187E) at 1066 MHz (for 1066 Mega-transfers/sec—up to 2 GB/sec) to allow for a soft-core CPU in the FPGA, as well as an additional memory buffer complementing the HMC.
5. 36 Mbit (2M x 18) QDRII+ Extreme SRAM memory chip (Cypress CY7C1263XV18) operating at 633 MHz to provide an additional 36 Mbits of SRAM with data transferred to/from the FPGA at 1266 MHz.
6. Soft-core CPU boot EEPROM.
7. FPGA configuration EPCQ-L devices, sized for containing two complete boot images for the largest-sized FPGA that can be accommodated by the footprint. These devices are configured via the MC2 JTAG port, in FPGA write-through mode.
8. Dual Micrel SY87701 CDR (Clock-Data Recovery) PLL devices to allow internal FPGA operations to be synchronized to an external clock, which may contain embedded timing information. These devices operate over a range from 32 MHz to 1250 MHz (32 Mbps, to 1.25 Gbps).
9. Programmable Zarlink ZL30160 PLL, used for providing the FPGA with SERDES reference clocks, either derived from an external source via the FPGA, a local reference 24.576 MHz LO, or one of the CDR PLL sources.
10. 125 MHz LO fed directly into the FPGA.
11. PowerMX MC2 I2C bus, as well as MC2 MCTx/Rx as per the PowerMX Base Specification.

[1] There are device variants—see Table 2-1.
[2] Which allow 16 SERDES I/Os to be migrated to 28 Gbps speeds.
[3] According to the HMC, V1.0 Specification.

12. Auxiliary MC3 A and B (A_aTx/Rx, B_aTx/Rx), and MCA A_CK* connection to APMX connectors for auxiliary data and clock to motherboard APMX connectors.
13. Auxiliary MCA: axCKi/o clocks to allow the module to be the source or receptor of these motherboard clocks. As the MC2: MCTx/Rx signals are not fed into FPGA SERDES CDR channels, these clocks could allow these lines to synchronize to these external motherboard-provided clocks.
14. 4 kbit 1-Wire EEPROM, as per Base Specification mandatory requirements.

Complete assembly names reflect variants of FPGAs actually mounted on this board. These variants can be device speed variants within one particular FPGA, and/or different FPGAs. These variants are identified in assembly names by appending the precise FPGA product code to the root product name. There is also an HMC variant (2GB or 4GB), contained within the root product name.

The format/nomenclature for these variants is as follows:

P32S-64M-*<2|4>***GB**: *<FPGA product code>*

Some examples are shown in Table 2-1:

Table 2-1 FPGA Variant naming.

Assembly name	Description
P32S-64M-4GB: 10AX900U1F45E2SG	4GB HMC; Arria GX 900, 96 SERDES, fastest transceivers, Extended operating temperature, mid-speed FPGA fabric, Standard power, RoHS6. **This is the standard device**.
P32S-64M-2GB: 10AT115U1F45I1SG	2GB HMC, Arria GT 1150, 96 SERDES, fastest transceivers (16 at 28 Gbps), Industrial operating temperature, fastest FPGA fabric, Standard power, RoHS6.
P32S-64M-4GB: <Stratix-10 product code>	TBD.

Refer to Altera documentation at www.altera.com for further information on migration compatibility with the Arria standard device

A block diagram of the board, containing the Arria GX900 standard device is shown in Figure 2-1.

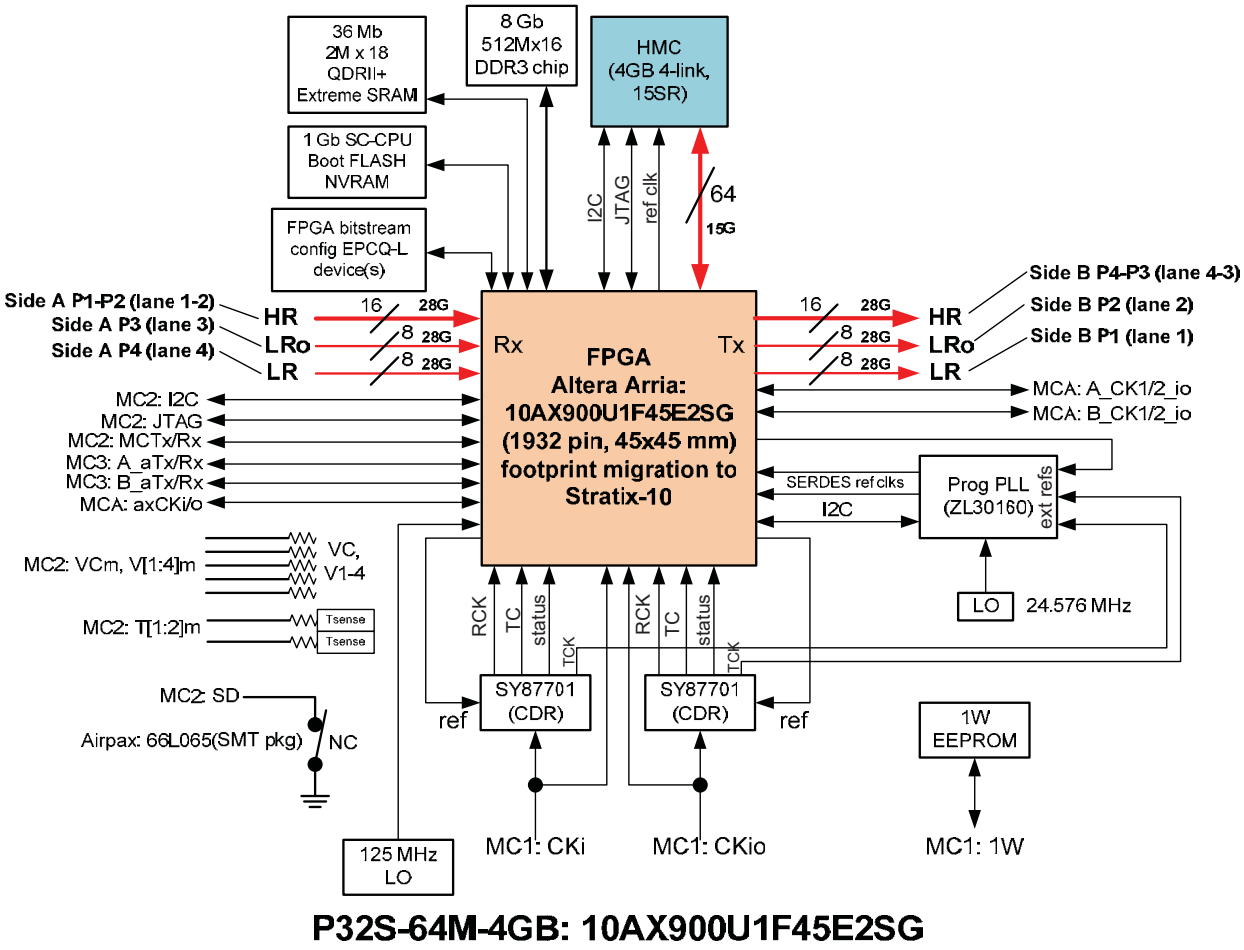

Figure 2-1 P32S-64M-4GB: 10AX900U1F45E2SG "standard device" block diagram.

The PMXM board layout is to be developed, but typically the FPGA, HMC, and most other functional components are mounted on the Front Side (refer to Figure 5-9 of the Base Specification), with connectors and support components mounted on the Rear Side as required.

3 Product Requirements

This section defines detailed product requirements, fleshed out as accurately as possible at this product definition stage but with further details to be worked out during detailed design. In all of the following requirements, "Base Specification" refers to [1], the PowerMX Base Specification. Unless otherwise noted, all section, table, and figure references in this section are to the Base Specification.

3.1 Functional Requirements

1. All mandatory requirements of the Base Specification, as they pertain to a PMXM plug-in module (physical, electrical, functional, reliability, PA, QA) apply unless otherwise noted in this specification. Inclusion of the MCA connector with connections to the FPGA according to Figure 2-1 of this product spec.
2. FPGA footprint for the Altera Arria 10AX900U1F45E2SG 45 x 45 mm device, with support in place as necessary for footprint compatibility with all Altera Arria and Stratix-10 devices as defined in Altera literature at www.altera.com.
3. 4-link HMC device, supporting 15 Gbps per lane (SERDES pair), requiring 64 FPGA SERDES transceivers. Pinout, footprint, functionality, and performance according to the HMC V1.0 Specification [2] SR (or USR if better/applicable as the FPGA and HMC are on the same card, as long as FPGA device migration requirements are met.) Suggested device is the Micron MT43A4G80100NFH-S15:A.
4. 96 SERDES connections as per Figure 2-1. Referring to Figure 2-1 this means:
    a. **HR** inputs and outputs are assigned to SERDES transceiver banks GXBL1H, GXBL1G, GXBL1F, and GXBL1E. These I/Os must use CH0, CH1, CH3, and CH4 within these banks. The inputs are assigned to Side A P1-P2 (lanes 1-2), 8 pairs each and must be the same 8 pairs in each P1, P2 (PMX12) connector. Transceiver outputs must be similarly assigned to P4-P3 pairs, with each transmitter matching the receiver's PMX12 pair assignment.
    b. **LRo** inputs and outputs, in Arria GT devices, use unusable transceivers within the above banks, when transceivers are operating in GT mode. i.e. transceivers CH2 and CH5. Similar requirements for transceiver to Side A and Side B PMX12 pair mapping.
    c. **LR** inputs and outputs use normal GX transceivers. Similar requirements for transceiver to PMX12 pair mapping.
    d. **64** GX transceivers allocated to the HMC links.
5. 8 Gbit (512k x 16) DDR3L memory chip attached to the FPGA, suggested part number is Micron MT41K512M16-187E.
6. 36 Mbit (2M x 18) QDRII+ Extreme SRAM memory chip attached to the FPGA, suggested part number is Cypress CY7C1263XV18.
7. Soft-core CPU boot FLASH memory with ability to be written/updated by the FPGA. Minimum 1 Gbit memory capacity, in x16 configuration. Suggested part is Numonyx PC28F00AP30TF. This FLASH memory is independent of the FPGA bitstream memory; the FPGA bitstream boots first, and if a soft-core CPU is present, the CPU boots its OS from this memory.

8. FPGA bitstream boot memory EPCQ-L and configuration to support booting of 2 complete and independent bitstreams, sized large enough to support all devices that are footprint compatible with the Arria GX 900 standard device, including Stratix-10. Use AS (Active Serial) x 4 configuration, with MC2:JTAG (from motherboard host SMC circuitry) write-through to write to the boot memory. After the memory is configured, the FPGA thereafter boots from memory, and may be instructed to switch boot images and reboot from the motherboard, either via the MC2:I2C bus, or the MC2:MCTx/Rx Gigabit Ethernet connection.
9. Dual Micrel SY87701 devices, connected as shown in Figure 2-1:
    a. MC1:CKi and MC1:CKio pins connected into each Micrel device, as well as directly into FPGA global clock pins.
    b. SY87701 recovered clock (CK) and data (TC) connected into the FPGA, the former into global clock pins.
    c. FPGA clock output pins connected into SY87701 ref inputs.
    d. SY87701 TCK outputs are additionally connected to the Zarlink PLL reference inputs, allowing these recovered clocks to act as a high precision reference for the FPGA.
10. Low jitter[4], 125 MHz +/-50 ppm LO fed into an FPGA global clock input. Suggest using a MEMs oscillator device for highest performance.
11. Zarlink ZL30160 programmable PLL, with low jitter 24.576 MHz +/-50 ppm, with TBD clock outputs fed into FPGA global clock and SERDES reference clock inputs. Suggest using a MEMs oscillator device for highest performance. The number of ZL30160 output clocks that are required, and which FPGA SERDES reference clocks they are routed to are TBD. FPGA output clock and SY87701 TCK outputs connected to Zarlink ref inputs. Zarlink I2C bus connections to the FPGA, to allow the FPGA to program the device.
12. 4 kbit 1-WIRE EEPROM, to meet mandatory Base Specification requirements. This is connected by 1 wire to the MC1:1W pin. An access method for factory programming this device when the module is not plugged into a motherboard, or connected to power must be provided. This device must contain information about the P32S-64M-4GB module, according to the Base Specification. The <module_product_name> must contain the assembly name according to section 2 and Table 2-1 of this specification, as well as version and manufacturer's name. NRC will provide precise EEPROM information to be written to the device by the manufacturer.
13. Direct JTAG connection from the FPGA to the MC2 connector as well as JTAG chaining of all other devices on the board that support JTAG (Boundary Scan Test).
14. VC, V1-4 voltage monitoring circuitry according to the Base Specification.
15. T[1:2]m temperature monitoring circuitry according to the Base Specification. One sensor must be closely thermally coupled[5] to the FPGA, and one must be thermally coupled and represent the PCB temperature.

[4] To support all possible SERDES speeds up to and including 28 Gbps.
[5] Direct mounting to the FPGA package is one possibility, however, a surface-mount sensor located as close as possible to the FPGA may be sufficient.

16. Thermal overload protection using the SD pin according to the Base Specification, and the circuit shown in Figure 2-1. The Airpax thermal protection device should be mounted on the PCB to be as thermally coupled to the FPGA as possible as it forms the “last-resort” thermal overload protection for the board.
17. Additional power supplies as needed, derived from V4, if not available as one of VC, or V1-V4.

3.2 Performance Requirements

1. All HR, LRo, and LR input and output PCB data paths must be designed and verified (through post-layout signal integrity modeling) for 28G/pair operation, as ultimately this will be possible with a Stratix-10 device.
2. The 64 transceivers to the HMC device must be designed and verified for 15G/pair operation.
3. PCB design and layout to meet all FPGA and surrounding devices speed and power supply tolerance and noise requirements. V1-V4 and V2 feedback paths chosen to ensure voltage tolerance requirements are met.

3.3 Other Requirements

1. Placement of all significant heat-dissipation devices on the Front Side of the PCB. Rear side placement of other components used where necessary, noting the maximum Rear Side component height restrictions in the Base Specification.

4 PCB Layout and Routing Considerations

A notional layout of the board showing the FPGA and the HMC device is shown in Figure 4-1.

It is expected that the following PCB traces and technologies will be required to meet performance requirements:

1. Megatron-6 material.
2. Blind and buried vias with backdrilling to 0.005” tolerance.
3. Anti-pads.
4. Removal of non-functional via pads on layers where no traces are routed.
5. Multi-layer microvias.

NRC’s signal integrity testing indicates that with proper design and materials, performance requirements can be met. Careful placement of power planes to avoid being adjacent to the highest-speed routing layers will likely be required. High-frequency filtering of V1-V4 and VC on entry to the board is likely important noting that the Base Specification places strict requirements on the quality of these voltages already.

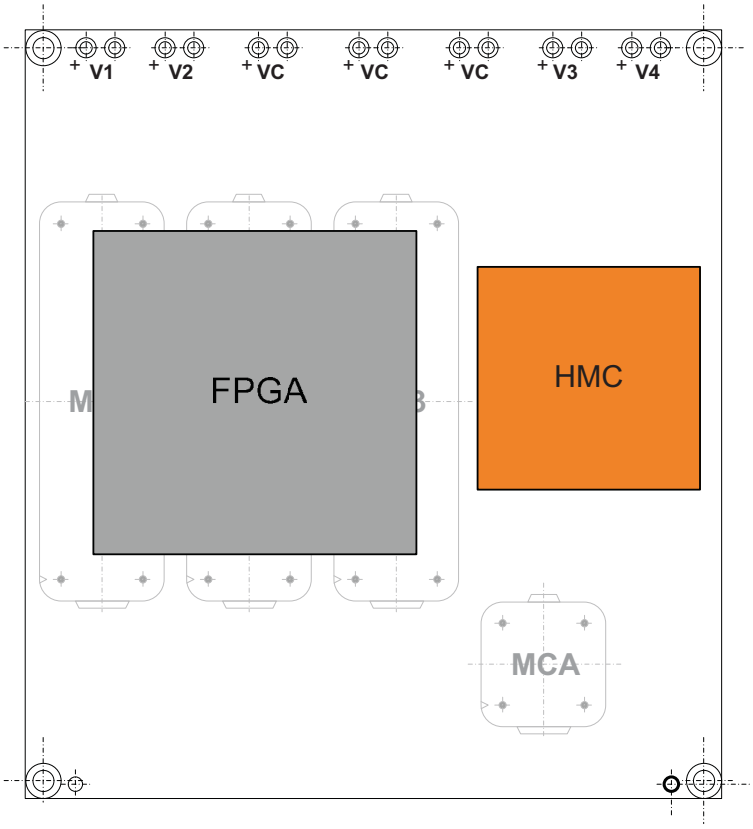

Figure 4-1 Notional PCB layout showing only the 45x45 mm FPGA and 31x31 mm HMC devices.

5 References

[1] PowerMX Base Specification, Version: Preliminary. See: http://www.powermx.org

[2] Hybrid Memory Cube Specification 1.0.

ANNEX D BASIS OF PAYMENT

Item	description	Firm Price CAD	Delivery date offered
1	Firm lot price for work provided under **MEX 4** project **As per statement of work: MEX4 SOW** The purpose of the MEX4 project is to fabricate representative physical models, containing electrical test coupons, of the PowerMX 4-site motherboard, PMXM module, and monolithic PMX_IOC. Each of these is to be fabricated according to the Base Specification, as further described in the next section on Product Build Descriptions.	$	
2	Firm lot price for work provided under **P32S** project **As per statement of work : P32S-64M-4GB SOW** PCB design, layout, routing, and cost analysis of the P32S. This includes progressing the hardware design complete to the point of being ready for prototype fabrication, as well as performing prototype and production cost analysis. NRC will provide PCB material, stackup, and trace/via geometry information (for high-speed SERDES channels) required to successfully design the board. NRC will perform post-layout signal integrity analysis of SERDES channels and all other traces to verify performance prior to prototype fabrication. * Subsequent phases for P32S project: The following is for information only at this stage. NRC may wish to amend any resultant contract issued to the successful bidder of the P32S project to include the following additional phases or at Canada's discretion, Canada may competitively tender the work under Phase 2 and or Phase 3. Phase 2: prototype fabrication and test. Phase 3: design iteration, re-prototype, pre-production fabrication.	$	